REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of November 20, 2002 is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Examiner has rejected claims 1-5 and 8 under 35 USC § 102(b) as being anticipated by the Cook reference (USP 4,997,775); and has rejected claims 6 and 7 as being unpatentable over the Cook reference in view of the Kawakatsu reference (USP 4,731,341). However, independent claim 1 has now been amended as indicated above. Therefore, for the reasons discussed below, it is respectfully submitted that amended independent claim 1, as well as the claims that depend therefrom, are clearly patentable over the prior art of record.

Independent claim 1 has now been amended to incorporate the subject matter of original dependent claims 2 and 5. In particular, amended independent claim 1 now recites that the base region is formed on the top surface of the collector layer *using epitaxial growth technology*. As explained in paragraph 18 on page 5 of the specification, by using epitaxial growth technology to form the base region, variation in the width of the base region can be significantly reduced as compared to semiconductor devices manufactured with conventional methods such as ion implantation or thermal diffusion.

The Cook reference discloses a method of forming a transistor, including a collector layer 16. The Examiner asserts that this reference also discloses a base region 66, 68 formed on the top surface of the collector layer 16 using epitaxial growth technology, and refers to column 3, lines 14-20 as support for this position. However, this section of the Cook reference only teaches that layer 14 and collector layer 16 of the transistor are epitaxially grown. In contrast to the Examiner's position, the Cook reference teaches that the base region 66 is formed by ion implantation, while base region 68 is formed by diffusion (see column 5, lines 9-24). In other words, the Cook reference merely teaches forming a base region in the conventional manner discussed in this application. Thus, contrary to the Examiner's assertion, the Cook reference does not disclose or suggest forming a base region of a

second conductivity type on a top surface of a collector layer of a first conductivity type, in which the base region is formed using epitaxial growth technology.

The Kawakatsu reference discloses a method of fabricating a semiconductor circuit including, the Examiner asserts, forming a bipolar transistor using an arsenic doped polysilicon emitter contact layer 116. However, the Kawakatsu reference also does not teach or suggest forming a base region of a second conductivity type on a top surface of a collector layer of a first conductivity type, in which the base region is formed using epitaxial growth technology. Therefore, one of ordinary skill in the art would not be motivated by the Kawakatsu reference to modify the Cook reference or to combine the references in a manner that would result in the invention recited in amended independent claim 1. Accordingly, it is respectfully submitted that amended independent claim 1 and the claims that depend therefrom are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The claims have been amended as follows:

1. (Amended) A method of manufacturing a semiconductor device, comprising:

forming a collector layer of a first conductivity type;

forming a base region of a second conductivity type formed on a top surface of said collector layer of said first conductivity type, said first conductivity type being opposite said second conductivity type, said base region being formed using epitaxial growth technology, and [said base region] being formed as a single region having a uniform depth[thereof];

forming a groove in a top surface of said base region at a portion thereof; [and]

forming spacers on sidewalls of said groove;

forming a diffusion source film in said bottom surface of said groove to be embedded therein between said spacers; and

forming an emitter region of said first conductivity type in said base region at a bottom surface of said groove, said emitter region being formed in said top surface of said base region at a bottom of said diffusion source film between said spacers.

6. (Amended) A method of manufacturing a semiconductor device according to claim [5] 1, further comprising:

forming a base electrode on said top surface of said base region around said portion of said groove; and

an emitter electrode on said surface of said diffusion source film.